The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHINNA PRUDVI and DEREK BACHAND

Appeal No. 2004-2039
Application No. 09/212,291

ON BRIEF[1]

Before JERRY SMITH, BLANKENSHIP, and NAPPI, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-7, 11-21, and 23-29, which are all the claims remaining in the application.

We affirm-in-part.

[1] Appellants waived an oral hearing via facsimile transmission January 18, 2005 (Paper No. 30).

BACKGROUND

The invention relates to a processing agent that may include an internal cache having a plurality of cache entries. Each cache entry may store multiple data line lengths of data. Claim 1 is reproduced below.

1. A processing agent to transfer data of a predetermined data line length in an external transaction, the agent comprising an internal cache having a plurality of cache entries, each entry sized to store multiple data line lengths of data.

The examiner relies on the following references:

Sachs et al. (Sachs)	4,884,197	Nov. 28, 1989
Scales, III et al. (Scales)	4,914,573	Apr. 3, 1990

Claims 24 and 29 stand rejected under 35 U.S.C. § 102 as being anticipated by Sachs.

Claims 17-21, 23, 27, and 28 stand rejected under 35 U.S.C. § 102 as being anticipated by Scales.

Claims 1-7, 11-16, 25, and 26 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sachs and Scales.

Claims 8-10 and 22 have been canceled.

We refer to the Final Rejection (Paper No. 18) and the Examiner's Answer (Paper No. 22) for a statement of the examiner's position and to the Brief (Paper No. 21) and the Reply Brief (Paper No. 23) for appellants' position with respect to the claims which stand rejected.

OPINION

Claims 24 and 29 -- Sachs

Appellants submit arguments in the Brief for claims in addition to those for claims 24 and 29, because the Final Rejection listed additional claims as being rejected. However, the examiner states in the Answer that only claims 24 and 29 are rejected under 35 U.S.C. § 102 as being anticipated by Sachs.

With respect to the subject matter of instant claim 24, appellants submit that the present invention defines a data line length to be the maximum length of data that may be transferred in a single bus transaction, referring to pages 1 and 2 of the application.

The instant specification, at pages 1 and 2, describes a particular bus protocol whereby up to 32 bytes of data may be transferred in a single bus transaction, and the processor contains an internal cache having cache entries of 32 bytes in length. Appellants have not pointed out, nor do we find, any clear statement defining "data line length" as the maximum length of data that may be transferred in a single bus transaction. The instant record is contrary to appellants' position. Claim 29 further limits base claim 24, in the requirement that "data line" corresponds to the maximum amount of data that can be transferred in a single bus transaction. Appellants' arguments, therefore, relate to the subject matter of claim 29, but are not commensurate with the scope of independent claim 24. Having not shown error in the rejection, we sustain the rejection of claim 24.

Further, we are not persuaded that instant claim 29 distinguishes over Sachs. Each cache line of Sachs contains four 32-bit words (i.e., a quadword), as shown in Figures 10A, 10B (col. 22, li. 14 et seq.). The rejection (Answer at 6) refers to column 6, line 27 et seq. for disclosure of the subject matter of claim 29. The section relates to transactions on data cache bus 131 (Fig. 1). Appellants argue (Brief at 8) that, at least at columns 10 and 14, Sachs teaches a sixteen-word transfer that can occur in a single bus transaction (on system bus 141; Fig. 1).

Figure 1 of Sachs also depicts intermediate bus 133, which couples data-cache MMU 130 to system bus 141. Col. 8, ll. 45-50; Fig. 6. System bus 141 allows single or multiple word block transfers. Col. 9, ll. 50-52. As appellants suggest, one cycle type calls for a 16-word transfer. Col. 10, ll. 24-33. Sachs refers to the 16-word transfers as "I/O type" cycles, but which may also serve in transfers to memory. Col. 13, ll. 12-13. Data transfer modes between data cache-MMU 130 to Main Memory 140 (Fig. 1) may be in a singleword or quadword mode. Block mode transfers may allow for a 16-word consecutive data transfer. Col. 15, ll. 24-45.

However, the examiner points to transfers on the data cache bus 131, which are limited to, at most, doubleword transactions (col. 6, ll. 45-58). Two doubleword transactions (two clock cycles), at a minimum, are required to load a quadword into a single cache line. Col. 23, ll. 11-23.

We thus agree with appellants to the extent that system bus 141 allows for up to 16-word transfers. However, instant claim 29 does not specify which bus, or "single bus

transaction," relates to the "maximum amount of data" that can be transferred. What a reference teaches is a question of fact. In re Baird, 16 F.3d 380, 382, 29 USPQ2d 1550, 1552 (Fed. Cir. 1994); In re Beattie, 974 F.2d 1309, 1311, 24 USPQ2d 1040, 1041 (Fed. Cir. 1992). Since appellants have not shown error in the examiner's findings, including that with respect to data cache bus 131, we sustain the rejection of claim 29.

Claims 17-21, 23, 27, 28 -- Scales

Instant claim 17 recites that when a data request misses the cache, a sequence of external transactions are posted to fill a cache line with data associated with the data request, wherein each cache line is sized to store multiple data line lengths of data.

According to appellants, Scales is directed to filling cache entries, rather than lines. As such, appellants argue that Scales fails to teach or suggest filling a cache line as claimed.

The examiner relies, in part, on column 1, lines 12 through 32 of the reference, which states that, typically in the art, operands are fetched from memory so as "to fill the entire cache line." Scale's invention relates to a solution to a problem in the prior art whereby if an operand, or portion thereof, is fetched that is insufficient in either size or alignment to fill an entire entry, then the operand is not cached at all.

In the system of Figure 1, the data bus 18 is 32-bits wide, but the bus master 12 and the system memory 16 are adapted to coordinate the transfer of byte (8-bit), word

(16-bit), and longword (32-bit) operands. The data bus 18 is longword aligned with respect to system memory 16, but the operands themselves may be aligned in system memory 16 on any byte boundary. Col. 2, ll. 10-28.

With respect to cache memory 22 (Fig. 2), each line of memory contains four longword entries. Id. at ll. 38-54. The reference goes on to detail adaptations whereby when a transferred operand is insufficient in either size or alignment to fill an entire entry, sufficient additional operands adjacent in system memory 16 are used to fill the entire entry in the cache line. Col. 2, l. 55 et seq.

Upon our review of the reference, we consider the examiner's position to be the more reasonable. Appellants indicate (Reply Brief at 3) that Scales "never" fills an entire cache line. On the other hand, the examiner finds (Answer at 20) that an entire cache line is filled whenever a sufficient number of cache entries are filled.

Considering the simplest case in Scales, in which all operands are longword (32-bit) and properly aligned, four cache entries in sequence fill an entire cache line, as the entries and lines are depicted in Figure 2. We consider it of no moment that Scales expresses, in the description of the invention, filling cache entries, rather than filling cache lines. As Scales notes, in typical operation, operands are fetched from memory so as to fill an entire cache line.

Moreover, we note that instant claim 17 does not require that in every instance when a request misses the cache, then a cache line is filled. The law of anticipation does not require that a reference "teach" what an applicant's disclosure teaches.

Assuming that a reference is properly "prior art," it is only necessary that the claims "read on" something disclosed in the reference, i.e., all limitations of the claim are found in the reference, or "fully met" by it. Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983).

Since appellants have not submitted separate arguments for the claims, and consistent with the rules in effect at the time of filing the briefs, claims 18-21, 23, 27, and 28 fall with representative claim 17. See 37 CFR § 1.192(c)(7) (1997).

Claims 1-7, 11-16, 25, and 26 -- Sachs and Scales

In response to the § 103 rejection over Sachs and Scales, appellants argue there is no motivation in the prior art for the proposed combination. Appellants point out that the cache memory of Sachs is organized on a quadword boundary. Col. 23, l. 11 et seq.; Fig. 12. Appellants further point to material at columns 26 and 27 of the reference and suggest that the reading or storing of words, halfwords, and bytes results in transactions with respect to an entire line (i.e., quadword) of cache memory. (Brief at 11.) As such, Sachs is not deemed to suffer from the problems of the prior art to which the system of Scales is directed (described at column 1, lines 28 through 33 of Scales).

In reply, the examiner repeats a somewhat vague statement of motivation with respect to "flexibility" and a "broader range of applications" (Answer at 22), but we do not find a satisfactory response from the examiner to appellants' argument. We thus are persuaded by appellants that a prima facie case for obviousness has not been

established on this record. We do not sustain the rejection of claims 1-7, 11-16, 25, and 26 under 35 U.S.C. § 103 as being unpatentable over Sachs and Scales.

CONCLUSION

The rejection of claims 24 and 29 under 35 U.S.C. § 102 as being anticipated by Sachs is affirmed. The rejection of claims 17-21, 23, 27, and 28 under 35 U.S.C. § 102 as being anticipated by Scales is affirmed. The rejection of claims 1-7, 11-16, 25, and 26 under 35 U.S.C. § 103 as being unpatentable over Sachs and Scales is reversed.

The examiner's decision in rejecting claims 1-7, 11-21, and 23-29 is thus affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a). See 37 CFR § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

JERRY SMITH
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

ROBERT E. NAPPI
Administrative Patent Judge

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